ECE354

1. Course number and name: ECE354 Digital Test

2. Credits and contact hours 2 credits; 2 contact hours.

3. Instructor's or course coordinator's name Jacob Savir

Text book, title, author and year P. H. Bardell et. al., "Built-in Test for VLSI: pseudorandom techniques", Wiley Interscience, 1987. ISBN 0-471-62463-2.

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   a. other supplemental materials: Class notes

4. Specific course information
   a. Catalog Description: Covers theory and practice related to test technology. Topics include fault modeling, test generation, fault simulation, design for testability, fault diagnosis, built-in self-test, scan design, and many others. Surveys several industrial design for testability structures.
   b. prerequisites or co-requisites: ECE 251 or equivalent, Math 333 or equivalent
   c. indicate whether a required, elective, or selected elective: required

5. Specific course learning outcomes (CLO):
   I. Student are able to a test set for a digital circuit.
   II. Student are able to apply design for testability techniques.
   III. Student are able to design LSSD and BIST into their product.
   IV. Student are able to compute test signatures.

   Relevant student outcomes (ABET criterion 3):

   (a) an ability to apply knowledge of mathematics, science, and engineering (CLO I, IV)
   (e) an ability to identify, formulate, and solve engineering problems (CLO II, III)
   (k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. (CLO II,IV)

6. Brief list of topics to be covered:

   Week 1: Introduction to test; review of Boolean algebra
   Week 2, 3: Test generation algorithms: Boolean difference; D-algorithm
   Week 4: Fault simulation: parallel, deductive, concurrent

Week 5: Scan design: LSSD
Week 6: BIST generators: LFSRs, primitive polynomials
Week 7: Signature collection: MISRs, aliasing probability
Week 8: Pseudorandom BIST theory: signal probability, detection probability, test length
Week 9: Parker-McCluskey algorithm, cutting algorithm, detection probability profile
Week 10: Logic modification; weighted random patterns
Week 11: Delay test: concept, two-pattern test, test length
Week 12: Industrial design-for-testability techniques
Week 13: BIST structures: ECIPT, STUMPS, BILBO
Week 14: Review