NJIT
ECE690: COMPUTER SYSTEMS ARCHITECTURE
COURSE SYLLABUS

Instructor: Professor S.G. Ziavras, ziavras@njit.edu, (973) 596-3462.
Office hours: By appointment (Graduate Studies Office, Fenster 140).
Description: This course deals with the design and performance evaluation of advanced/high-performance computer systems. The emphasis is on microprocessors, chip-multiprocessors and memory hierarchy design. Historical information is presented as well along with data storage and low-power dissipation schemes. Special attention is paid to pipelining, ILP (instruction-level parallelism), DLP (data-level parallelism) and TLP (thread-level parallelism) using hardware) and/or software techniques to yield high performance.
Prerequisites: Undergraduate degree in Computer Engineering, or ECE 684 or equivalent.
Textbook: *Computer Architecture: A Quantitative Approach*, by John L. Hennessy and David A. Patterson, Morgan Kaufmann, 5th edition, 2011, ISBN: 9780123838728.
Lecture notes and other references: http://web.njit.edu/~ziavras/classes.htm

Learning outcomes:
- Understand the inner workings and performance capabilities of advanced microprocessors.
- An ability to evaluate hardware accelerators targeting at applications with substantial data-level parallelism (DLP).
- Learn software-driven techniques to match application requirements to available pipelined hardware in order to obtain high performance.
- An ability to estimate the static and dynamic power dissipation of given hardware modules.
- An ability to design microprocessor-based systems by accounting for performance and power dissipation.
- An ability to anticipate hardware performance improvements based on established rules from past experiences with computer technology.
- Improve report-writing skills when presenting results for computer design and evaluation.
- Learn the differences among multiscalar, superpipelined, multithreaded, simultaneous multithreaded, vector, and multicore processors.
- Understand the forces behind the computer industry's shift to multicore processors.
- Understand cache coherence issues.
- An ability to design advanced memory hierarchies.
- Understand the basic differences between shared-memory and message-passing interprocessor connection networks.
- An ability to select appropriate computer systems for given application domains.
- Understand what hardware and software problems will require solutions for future generations of multicore processors targeting at thread-level parallelism (TLP) and heterogeneous systems.

COURSE OUTLINE

Weeks	Chapter
1-3	Chapter 1: Fundamentals of Quantitative Design and Analysis (Sections 1.1-1.9) Appendix A: Instruction Set Principles (Sections A.1-A.10)
4-5	Appendix C: Pipelining: Basic and Intermediate Concepts (Sections C.1-C.5)
6-7	Appendix B: Review of Memory Hierarchy (Sections B.1-B.3) Chapter 2: Memory Hierarchy Design (Section 2.1)
8	**MIDTERM EXAM**
9-10	Chapter 3: Instruction-Level Parallelism and Its Exploitation (Sections 3.1-3.12)
11-12	Chapter 5: Thread-Level Parallelism (Sections 5.1-5.6)
13-14	Chapter 4: Data-Level Parallelism in Vector, SIMD, and GPU Architectures (Sections 4.1-4.4) **Week 14: Project report due**

Grading Policy:

Midterm exam:	35%	(2 hours, open book, open notes)
Final exam	35%	(2 hours, open book, open notes)
Project:	30%	(report due in week 14)

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