ECE689
Computer Arithmetic Algorithms
NJIT ECE
Wednesday 6:00pm-9:05pm

Official Prerequisite: Undergraduate course in logic design
Recommended prerequisite: Computer Organization/Architecture courses

Official Course Catalog Description:
Data representation, integers, floating point and residue representation. Bounds on arithmetic speed, algorithms for high speed addition, multiplication, and division. Pipelined arithmetic. Hardware implementation and control issues.

Expanded Description:
The purpose of this course is to provide both the theory and practice of state-of-the-art algorithms and designs for arithmetic operations. Computer arithmetic is a subfield of digital computer organization. It deals with the hardware realization of arithmetic functions to support various computer architectures as well as with arithmetic algorithms for firmware/software implementation. A major thrust of digital computer arithmetic is the design of hardware algorithms and circuits to enhance the speed of various numeric operations. Thus much of what is presented in this course complements the architectural and algorithmic speedup techniques covered as part of the advanced computer architecture courses.

Textbook:
Computer Arithmetic Algorithms, 2nd Edition,
by Israel Koren,
published by A. K. Peters, Natick, MA, 2002 (ISBN 9781568811604)

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Office Hours: Wednesday 5pm-6pm; and by appointment
Location: Room 324 ECEC, or in the classroom
Telephone: 973-596-5692

LiveMeeting: In case of snow or any reason that in-class presence is not permitted, we shall use LiveMeeting. LiveMeeting notice and conference call number will be broadcast by email and posted on NJIT Moodle

Any student who has a need for accommodation based on the impact of a disability should contact me privately to discuss the specific situation as soon as possible.

Grading Policy:

No late assignments will be accepted!
No cheating and plagiarisms will be tolerated!

Written Homework Assignments	
Written HW after each chapter	**0%,** for practice only
Reading Assignments and write-ups	
Seven papers and write-ups	**15%**
Quizzes (close book, but your own 1-page summary sheet, your own written HW assignments, and your own reading write-ups are allowed)	
Two Quizzes	**50%** (25% each)
~~Final Exam (open book, comprehensive)~~	~~**24%**~~
Term Project (individual or pair)	**35%**

Suggested types of final projects:

- Hardware implementation (in Verilog or VHDL) of an arithmetic unit/algorithm;
- Software simulation (in C or Java) of an arithmetic unit/algorithm;
- Research study of a novel or published arithmetic unit/algorithm.

Topics Covered:

Number systems.
- **Chap 1.** Conventional number
- **Chap 2.** Unconventional fixed-radix number systems.

Residue numbers and its arithmetic.
- **Chap 11.** The residue number system

Limits of fast arithmetic.

Fixed-point addition and subtraction.
- **Chap 5.** Algorithms for fast addition.

Floating-point addition and subtraction.
- **Chap 10.** Logarithmic number systems
- **Chap 4.** Floating-point arithmetic

Fast multiplication
- **Chap 3.** Sequential algorithms for multiplication and division.
- **Chap 6.** High-speed multiplication.

Fast division.
- **Chap 7.** Fast division
- **Chap 8**. Division through multiplication.

Elementary functions.
- **Chap 9.** Efficient algorithms for evaluation of elementary functions.

Pipelined arithmetic.

Reading Assignments:

1. Number Systems
   Vergos, H.T.; Dimitrakopoulos, G.; , "On Modulo 2^n+1 Adder Design," *Computers, IEEE Transactions on* , vol.61, no.2, pp.173-186, Feb. 2012
2. Addition/Subtraction

V. Kantabutra, "A Recursive Carry-Lookahead/Carry-Select Hybrid Adder," *IEEE Trans. Computers*, Vol. 43, No. 12, pp. 1495-1499, December 1993.

3. Multiplication
   J. M. Jou, S. R. Kuang, and R. D. Chen, "Design of Low-Error Fixed-Width Multipliers for DSP Applications," *IEEE Trans. Circuits and Systems II*, Vol. 46, pp. 836-842, June 1999.
4. Division
   Focus on the section "New Radix-16 Divider" on p.186
   J. Coke, H. Baliga, N. Cooray, E. Gamsaragan, P. Smith, K. Yoon, J. Abel and A. Valles, "Improvements in the Intel® Core™2 Penryn Processor Family Architecture and Microarchitecture", Intel Technology Journal, Vol. 12, Issue 03, October 2008
5. Real Arithmetic
   A. Eisinberg and G. Fedele, "Accurate Floating-Point Summation: A New Approach," *Applied Mathematics and Computation*, Vol. 189, pp. 410-424, 2007.
6. Elementary Functions.
   T. Sasao, S. Nagayama, and J. T. Butler, "Numerical Function Generators Using LUT Cascades," *IEEE Trans. Computers*, Vol. 56, No. 6, pp. 826-838, June 2007.
7. Pipeline Arithmetic/GPU Computing
   K. Fatahalian, J. Sugerman, and P. Hanrahan. 2004. "Understanding the efficiency of GPU algorithms for matrix-matrix multiplication." *In Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware*

Homework Assignments:

- Assignment #1: Chapter 1, Problems 1, 2, 5, 6, 7, 8, 9 and 13.
- Assignment #2: Chapter 2, Problems 1, 2, 5, 7, 10 and 12.
- Assignment #3: Chapter 3, Problems 1, 2, 3, 4, 6, 8 and 10.
- Assignment #4: Chapter 4, Problems 2, 3, 4, 10, 11, 12, 14 and 16.
- Assignment #5: Chapter 5, Problems 2, 3, 4, 6, 9 (should be Fig. 5.8 rather than 5.5), 12, 13, 15, 17, 18 and 20.
- Assignment #6: Chapter 6, Problems 4, 7, 8, 11, 12, 13 and 14 or 15.
- Assignment #7: Chapter 7, Problems 2, 4, 5, 10, 11 and 13.
- Assignment #8: Chapter 8, Problems 3, 8 and 9.
- Assignment #9: Chapter 9, Problems 1, 2 and 6.

Tentative Schedule:

Lecture	*Topics*
1	Introduction
	Number systems
	HW
[1/28 last day to add/drop a class]	
2	Number systems
	Residue numbers and its arithmetic
	HW
3	Unconventional number systems
	Limits of fast arithmetic
	Paper#1 write-up due
	HW
4	Unconventional number systems
	Fixed-point addition and subtraction
	HW

	Paper#2 write-up due
5	**Quiz #1**
	HW
6	Fixed-point addition and subtraction (continued)
	HW
	Paper#3 write-up due
7	Fixed-point addition and subtraction (continued)
	Start your planning for Term Project
8	Floating-point addition and subtraction
	HW
	Paper#4 write-up due
9	Fast division (continued)
	Term Project proposal due and short presentation of each team
	Paper#5 write-up due
10	**Quiz #2**
	Elementary functions
	HW
11	Elementary functions (continued)
	Paper#6 write-up due
12	Pipelined arithmetic
	HW
	Term Project progress check-point meetings
13	Pipelined arithmetic (continued)
	Paper#7 write-up due
14	**Final Exam**
15	**Term Project Presentation & Report due**