	Department of Electrical and Computer Engineering
Course	ECE 452 - Design Advances in Computer Architecture (3 credits)
Instructor	Dr. Bipin Rajendran Phone: x3516, Office: ECE Bldg., Room 337 Email: bipin@njit.edu
Text Books The fo	 Ilowing reading materials based on Synthesis Lectures that are available online for NJIT users for free will be used as text material. Also relevant papers published in top-tier conferences will be provided in the class. 1. Bruce Jacob, The Memory System, Synthesis Lectures on Computer Architecture, M&C , 2009
	 Daniel J. Sorin, Fault Tolerant Computer Architecture, Synthesis Lectures on Computer Architecture, M&C, 2009
	 Moinuddin K. Qureshi, Sudhanva Gurumurthi, Bipin Rajendran, Phase Change Memory: From Devices to Systems, Synthesis Lectures on Computer Architecture, M&C, 2011
	 G. Indiveri and SC. Liu, Memory and information processing in neuromorphic systems, Proceedings of the IEEE, Dec 2015
	 Hyesoon Kim, Richard Vuduc, Sara Baghsorkhi, Jee Choi, Wen-mei Hwu, Per- formance Analysis and Tuning for General Purpose Graphics Processing Units (GPGPU), Synthesis Lectures on Computer Architecture, M&C, 2012
	 Natalie Enright Jerger, Li-Shiuan Peh, On-Chip Networks, Synthesis Lectures on Computer Architecture, M&C, 2009
	M&C - Morgan & Claypool Publishers
Course Description	Overview of recent advances and topics of current active research in Computer Architecture. Includes: new computing paradigms such as brain inspired non- von Neumann architectures; stochastic computing; hybrid memory systems and other architectures leveraging emerging memory technologies; systolic array systems; new interconnect architectures including NoCs; GPU-accelerated computing etc.
Prerequisite	ECE 451
Specific course learning outcomes (CLO)	The student will be able to 1. Understand basic principles of non-Von Neumann computer architecture, and explain differences with Von Neumann architecture based on examples and design of brain-inspired systems
	 Understand and utilize the basic principles of stochastic computing architecture to analyze trade-o s with deterministic systems; design hardware modules and evaluate performance;
	 Quantitatively evaluate and compare design of hybrid memory systems that are based on emerging memory technologies with conventional memory hierarchy;
	 Understand and outline high level aspects of emerging topics such quantum computing, systolic array architectures, NoC design and General Purpose GPU programming paradigms.
	Read critically and analyze papers published in top-tier computer architecture conferences and journals.

(1) an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1)

(2) an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors. (CLO 2, 3, 4)

(3) an ability to communicate effectively with a range of audiences (CLO 5)

4) an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts. (CLO 1, 2, 3, 4)

(6) an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLO 2, 3)

(7) an ability to acquire and apply new knowledge as needed, using appropriate learning strategies (CLO 1,2, 3, 4)

Computer assisted design and course specific software	MATLAB, VHDL
Tentative Course Schedule	Week 1: Von Neumann vs Non Von Neumann Week 2-3: Principles of Brain-inspired Computing Week 4-5: Brain-inspired chip Architecture Week 6-7: Stochastic Computing principles & Architecture Week 8: Conventional Memory & Storage Hierarchy Week 9: Emerging Memory technologies Week 10: Hybrid Memory architectures Week 11: Systolic array architecture and examples Week 12: Quantum computing principles arch Week 13: Networks on chip - design and architectures Week 14: GPU architectures & acceleration
Grading	Final letter grade will be based on the following tentative curve: Homework + Quizzes & Class Participation - 20% Programming assignments/mini-projects - 25% Midterm Exam - 25% Final Exam - 30%
Honor Code	The NJIT Honor Code will be upheld; any violations will be brought to the immediate attention of the Dean of Students.