Hellen and John C. Hartmann Department of Electrical and Computer Engineering
New Jersey Institute of Technology

ECE 452-002 Advanced Computer Architecture II: **3.0 credits**
Instructor: Timothy Steele. **E-mail**: timothy.steele@njit.edu **Phone**: 973-596-3539
Textbook: William Stallings, *Computer Organization and Architecture, Designing for Performance, Ninth Edition***,** Prentice Hall, 2013

Course Description: Overview of recent advances and topics of current active research in the field of Computer Architecture. Includes: new computing paradigms such as brain inspired non-von Neumann architectures, stochastic computing, hybrid memory systems and other architectures leveraging emerging memory technologies. Systolic array systems; new interconnect architectures including NoCs; GPU-accelerated computing etc. are also discussed.

Course Description: Topics include memory allocation, single-instruction stream parallelism, parallelism by message passing, shared-resource systems, protection and security, stack-oriented systems, systolic array systems, and data-flow systems. Discusses the relationships between software and hardware levels of system implementation and -operation.
Prerequisite: ECE 451

Course Learning Outcomes
Upon successfully completing the course a student is able to:

#	Outcome
1	Describe the allocation and hierarchical organization of system memory.
2	Define and design for single instruction stream parallelism.
3	Define and design for parallelism in message passing architectures.
4	Define and design for shared resource systems.
5	Define and design for protection and security.
6	Define and design for stack oriented systems.
7	Define and design for systolic array systems.
8	Define and design for data flow systems.

ABET Criterion 3 Student Learning Outcomes

1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1-8);
5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives (CLO 1-8)
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLO 1-8)

Schedule:

Week	Topics	Book Sections

1-3	Memory organization and hierarchy	Chapters 4, 5 and 6, Appendix C,

		D, E and F
4	Memory allocation	Chapter 8
5-6	Instruction-level parallelism and recursion.	Chapter 16, Appendix H
7	Exam 1	
8-9	Parallel processing and systolic arrays.	Chapter 17
10	Multi-core computers	Chapter 18
11	Exam 2	
12	Stack oriented computers	Appendix O
13	Protection and security.	
14	Data flow systems	

Homework Policy
The list of problems for each assignment is posted to Moodle. A significant number of problems are assigned each week. They consist of questions from the text.

Grading Policy

1. Homework 10%
2. Exam 1 30%
3. Exam 2 30%
4. Final Exam 30%

Tests and final exam are closed book and notes. Students are allowed a single sheet of paper (front and back) containing formulas but no circuit diagrams or solved problems. Test grading: Full credit – for a detailed correct solution showing all steps. Partial credit – for partial answers. Answers with no work (even if correct) will receive minimal or no credit.

Honor Code
The NJIT Honor Code will be upheld, and any violation with be brought to the immediate attention of the Dean of Students.