Hellen and John C. Hartmann Department of Electrical and Computer Engineering
New Jersey Institute of Technology

ECE 452-002 Design Advances in Computer Architecture: 3.0 credits
Instructor: Timothy Steele. E-mail: timothy.steele@njit.edu Phone: 973-596-3539
Office Hours: Wednesday 5:00-6:00 PM, or by appointment (e-mail). Room ECEC 310
Course Description: Topics include memory allocation, single-instruction stream parallelism,
parallelism by message passing, shared-resource systems, protection and
security, stack-oriented systems, systolic array systems, and data-flow
systems. Discusses the relationships between software and hardware
levels of system implementation and -operation.
Prerequisite:
ECE 451

Course Learning Outcomes
Upon successfully completing the course a student is able to:

<table>
<thead>
<tr>
<th>#</th>
<th>Outcome</th>
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<tbody>
<tr>
<td>1</td>
<td>Describe the allocation and hierarchical organization of system memory.</td>
</tr>
<tr>
<td>2</td>
<td>Define and design for single instruction stream parallelism.</td>
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<tr>
<td>3</td>
<td>Define and design for parallelism in message passing architectures.</td>
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<tr>
<td>4</td>
<td>Define and design for shared resource systems.</td>
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<tr>
<td>5</td>
<td>Define and design for protection and security.</td>
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<tr>
<td>6</td>
<td>Define and design for stack oriented systems.</td>
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<tr>
<td>7</td>
<td>Define and design for systolic array systems.</td>
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<tr>
<td>8</td>
<td>Define and design for data flow systems.</td>
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ABET Criterion 3 Student Learning Outcomes

1. An ability to identify, formulate, and solve complex engineering problems by applying
   principles of engineering, science, and mathematics (CLO 1-8);
5. an ability to function effectively on a team whose members together provide leadership, create
   a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
   (CLO 1-8)
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and
   use engineering judgment to draw conclusions (CLO 1-8)

Schedule:

<table>
<thead>
<tr>
<th>Week</th>
<th>Topics</th>
<th>Book Sections</th>
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<tbody>
<tr>
<td>1-3</td>
<td>Memory organization and hierarchy</td>
<td>Chapters 4, 5 and 6, Appendix C,</td>
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Sequence

<table>
<thead>
<tr>
<th></th>
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<th>D, E and F</th>
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<tbody>
<tr>
<td>4</td>
<td>Memory allocation</td>
<td>Chapter 8</td>
</tr>
<tr>
<td>5-6</td>
<td>Instruction-level parallelism and recursion.</td>
<td>Chapter 16, Appendix H</td>
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<tr>
<td>7</td>
<td>Exam 1</td>
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<tr>
<td>8-9</td>
<td>Parallel processing and systolic arrays.</td>
<td>Chapter 17</td>
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<tr>
<td>10</td>
<td>Multi-core computers</td>
<td>Chapter 18</td>
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<tr>
<td>11</td>
<td>Exam 2</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Stack oriented computers</td>
<td>Appendix O</td>
</tr>
<tr>
<td>13</td>
<td>Protection and security.</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Data flow systems</td>
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**Homework Policy**

The list of problems for each assignment is posted to Moodle. A significant number of problems are assigned each week. They consist of questions from the text.

**Grading Policy**

1. Homework 10%
2. Exam 1 30%
3. Exam 2 30%
4. Final Exam 30%

Tests and final exam are closed book and notes. Students are allowed a single sheet of paper (front and back) containing formulas but no circuit diagrams or solved problems. Test grading: Full credit – for a detailed correct solution showing all steps. Partial credit – for partial answers. Answers with no work (even if correct) will receive minimal or no credit.

**Honor Code**

The NJIT Honor Code will be upheld, and any violation with be brought to the immediate attention of the Dean of Students.