New Jersey Institute of Technology

Electrical and Computer Engineering

Course Outline ECE 252 [**Microprocessors**]

Instructor: Azeez Bhavnagarwala

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Class Lecture: **Tuesdays 6:00 PM – 8:50 PM,** *Room:* **CULM LECT 2**

Office hours: **Tuesdays 4PM-5:30 PM** (Room: 342, ECE Building, Tel: 973-596-3663) or by appointment

Course Pre-requisites: Digital Design and Computer Organization (ECE 251) is required. Please see instructor if you have an equivalent background.

Summary Course Description: ECE 252 introduces students to Microcontrollers and the trends that are shaping their design and use – markets for billions of pervasive, low cost, connected and energy efficient IoT systems. ECE 252 focusses on the RISC V instruction set architecture (ISA) - an 'open source' ISA that enables IoT systems to deliver on three key capabilities: improved interoperability among vendors, higher performance, energy efficiency and a much lower cost than systems built with proprietary architectures – ARM, x86 etc. ECE 252 reviews the basic organization of and components used by the processor and details the ISA with its encoding, formats and extensions. The class reviews the RISC V memory map and the RISC V GPIO complex that manages the connection of digital I/O pads to digital peripherals, including SPI, UART, and PWM controllers, as well as for regular programmed I/O operations. ECE 252 also develops the background for students to pursue ECE 395 (Microprocessor Lab) with use of an online RISC V simulator, an introduction to the Arduino Integrated Development Environment and an introduction to IoT system design

Course structure:

Your performance in the course will be assessed with your performance in **weekly assignments** (30% of total grade), that include RISCV simulations, design problems and a review of a relevant assigned publications, **Two Quizzes** (20% of total grade each) and a **final** (30% of total grade). In addition, there will be a 2-week long **Term Project** that carry the weight of 2 HW assignments, Participation in these activities is highly encouraged.

Course Textbook:

John Hennessey & David Patterson, *Computer Organization & Design, The Hardware Software Interface*, RISCV edition

Course Learning Outcomes

I Be able to quantitatively *compare performance & energy efficiency* of different computers, ISAs and hardware implementations for a given workload and assess best opportunities for improving performance

II Understand and be able to use the RISC V ISA – formats, encoding, extensions. Integrate mastery of RISCV ISA Term project into Group Presentations to class on 11/26

III Understand and be able to use the RISC V memory map and the RISC V GPIO complex that manages the connection of digital I/O pads to digital peripherals, including SPI, UART, and PWM controllers, as well as for regular programmed I/O operations. Be able to use an online tool to program a RISC V controller.

Student Outcomes

1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO I, II, III)
2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (CLO I, II, III)
3. an ability to communicate effectively with a range of audiences (CLO I, II)
5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives (CLO I, II)
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLO I, II, III)
7. an ability to acquire and apply new knowledge as needed, using appropriate learning strategies. (CLO I, II, III)

Course Schedule:

Week	ECE 242 Content	Assignments
1	Computer Abstractions & Technology	HW 1
2	Introduction to RISC V & Basic Organization	HW 2
3	RISC V Instructions	HW 3
4	RISC V Instruction Formats	HW 4
5	**Quiz 1**	
6	Floating Point Arithmetic and IEEE 754 representation	HW 6
7	Floating Point Instructions and Hardware implementation	HW 7
8	Register and Calling Conventions, Compressed Instructions	HW 8
9	Memory Hierarchy & RISC V Memory Map	HW 9
10	**Quiz 2**	
11	Privilege modes & Virtual Memory	HW 10
12	Communication interfaces, GPIO, SPI, UART, and PWM controllers	HW 11
13	**Term Project Due, Group Presentations in Class**	
14	**Review Problem Sets for Final**	**Final Exam: Dec 17th**

Academic Integrity:

"Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are

working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: http://www5.njit.edu/policies/sites/policies/files/academic-integrity-code.pdf.

Please note that it is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. ***Any student found in violation of the code by cheating, plagiarizing or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university.*** *If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at dos@njit.edu"*