Helen and John C. Hartmann Department of Electrical and Computer Engineering New Jersey Institute of Technology

Course Number and Title: ***ECE 251. Digital Design. 3 credits, 4 contact hours***

Course Instructor: Jacob Savir
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Course description:

The design of combinational and sequential logic circuits used in digital processing systems and computers. Basic register transfer operations are covered. Topics include Boolean algebra, minimization techniques and the design of logic circuits such as adders, comparators, decoders, multiplexers, counters, arithmetic logic units, and memory systems.

Prerequisites: PHYS 122.

Text book*:* Alan B. Marcovitz, Introduction to Logic Design, 2nd edition (or higher), McGraw-Hill, ISBN # 0-07-286516-4.

Other supplemental materials: Class notes

Specific Course Learning Outcomes (CLO): The student will be able to

1. use Boolean Algebra.
2. minimize Boolean functions.
3. design digital circuits with gates, latches and flip flops; explain the design details
4. analyze digital circuit in a multitude of possible applications.

Relevant student outcomes (ABET criterion 3):

1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1-4)
2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (CLO 3)
3. an ability to communicate effectively with a range of audiences (CLO3)
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLO 3-4)

Brief list of topics to be covered:

Week 1: Number systems: decimal, binary, arbitrary radix representation.
Week 2: Representation of positive & negative numbers. Two's complement, One's complement, signed-magnitude, Hex, Octal, Ternary. Quick conversion between bases.
Week 3: Gates, truth tables, Boolean algebra, Function simplification.
Week 4: K-maps. Circuit implementation using K-maps. SOP and POS representation. NAND/NOR implementations.
Week 5: Mux, Demux, decoders, code conversion (BCD to Binary, Excess 3 to binary).
Week 6: Hazards, hazard-free design.
Week 7: Function implementation using MSI logic. Week 8: Latches and Flip-flops: SR, D, JK, T.
Week 9: Counter design, register design, ALU function.
Week 10: Sequential circuits. Excitation function, state table, state diagram. Week 11: Sequential circuit design with different flip-flops.
Week 12: Asynchronous circuits analysis and design. Excitation function, Flow table.
Week 13: PLDs, ROMs, PLAs, PALs.
Week 14: Review.

Grading policy: quizzes midterm examination and final examination

Updates and Assignments to be distributed via e-mail

Office hours, recitations and group studies: TBA

Honor Code: The NJIT Honor Code will be upheld; any violations will be brought to the immediate attention of the Dean of Students.