Ph.D Dissertation Proposal Defense

Candidate: Anakha Vasanthakumaribabu
Date: August 28, 2018
Time: 9 AM-10 AM
Venue: ECEC 202
Title: Efficient Hardware Implementation of Bio-inspired Networks

Abstract

Human brain with its computational capability and power efficiency has inspired today's popular machine learning algorithms. Deep Neural Networks (DNNs) have shown unprecedented success in many applications such as social media and business analytics, bio-informatics etc. DNNs use memoryless models of neurons whose output is determined only by the current stimuli. Unlike DNNs, third generation Spiking Neural Networks (SNNs) operate on discrete events in time called spikes, which are generated by the time integration of previous inputs, closely mimicking biological neurons. However, the major challenge faced by these artificial neural networks is their large training times on traditional von-Neumann machines. Hence, there has been significant efforts to build dedicated hardware to adopt large scale machine learning algorithms for embedded applications.

Several non-von Neumann architectures have been explored for accelerating DNN training and among these, implementations employing non-volatile memory (NVM) based electrical synapses are the most promising due to its area and power efficiency. However these NVM devices are non-ideal and hence, in the first part of our work, we explore the impact of experimental memristive characteristics in the stochastic learning of DNNs. We also study emerging memory devices to understand the device and architectural level optimizations necessary for obtaining reliable network performance.

In the second part of our work, we focus on SNN based machine learning algorithms which may be more ideally suited for building power efficient hardware due to the sparsity of spike based communication protocols. Promising results have been recently obtained for learning in SNNs using probabilistic neuron models. We study the optimization of these probabilistic algorithms for implementation in digital CMOS hardware.

After discussing the results obtained so far, I will summarize the future directions of our work including metrics for evaluation of these cognitive computing systems based on DNNs and probabilistic SNNs using digital CMOS as well emerging nanoscale memristive devices.

Committee members:

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Publications

1. A. V. Babu, B. Rajendran, Stochastic Deep Learning in Memristive Networks, 24^{th} IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2017.

2. A. V. Babu, S. Lashkare, U. Ganguly, B. Rajendran, Stochastic Learning in Deep Neural Networks Based on Nanoscale PCMO Device Characteristics, under review at Elsevier Journal on Neurocomputing.

3. S. R. Kulkarni, A. V. Babu, B. Rajendran, Acceleration of Convolutional Spiking Neural Networks using Memristive Devices, accepted at 19^{th} International Conference on Engineering Applications of Neural Networks (EANN), 2018.

4. S. R. Nandakumar, S. R. Kulkarni, A. V. Babu and B. Rajendran, Building Brain-Inspired Computing Systems: Examining the Role of Nanoscale Devices, IEEE Nanotechnology Magazine, August 2018.

5. S. R. Kulkarni, A. V. Babu, B. Rajendran, Spiking Neural Networks - Algorithms, Hardware Implementations, and Applications, IEEE 60th International Midwest Symposium on Circuits and Systems, 2017.