# ECE 495 Fall 2014
# Computer Engineering Design Laboratory

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| **Course Description:** | This course emphasizes hardware design and debugging. Topics include combinational and sequential logic design using CAD tools, VHDL, and design based upon PLA/PLD. |
| **Instructor:** | Dr. Edwin Hou<br>357 ECEC, (973) 596-3521<br>hou@njit.edu |
| **Lecture/Laboratory meet at:** | W 1:00pm-2:25pm (319 FMH) / M 10:00am-2:25pm (211A FMH) |
| **Office hours:** | R 1:30pm-2:30pm or by appointment |
| **Prerequisites:** | ECE 353 and ECE 394 |
| **Text:** | J. Knoots, E. Hou, Laboratory and Supplementary Notes,<br>ECE 495: Computer Engineering Design Laboratory, Ver. 3.0, ECE Dept. 2007.<br>**You will also need the Lab kit for ECE 394**.<br><br>S. Yalamanchili, *VHDL Starter's Guide*, Prentice Hall, 1998. |
| **Honor code:** | The NJIT honor code will be upheld and that any violations will be brought to the immediate attention of the Dean of Students. |

**Course Learning Outcomes (CLO):**

Student should be able to
1. design sequential circuits (using EEPROM) that meets a given design specification
2. use CAD tools to design, implement and verify their hardware system designs.
3. design hardware system and write VHDL program to implement them.
4. write lab reports documenting the results of the lab experiments.

**Relevant ABET Student Outcomes:**

(b) an ability to design and conduct experiments, as well as to analyze and interpret data; (CLO 1, 2, 3)
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability; (CLO 1, 2, 3)
(e) an ability to identify, formulate, and solve engineering problems; (CLO 1, 2, 3)
(g) an ability to communicate effectively; (CLO 4)
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice; (CLO 1, 2, 3)

**Grading Policy**

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| Quizzes & Final: | 15% | |
| Lab.: | 65% | |
| Demo | 40% | |
| Report | 25% | Writing (10%) |
| | | Logic Diagram (5%) |
| | | Wiring Diagram (2.5%) |
| | | Software/Code comments (5%) Timing Diagram (2.5%) |
| Pre-Lab: | 20% | Logic Diagram/Tables (5%) Wiring Diagram (5%) Software/Code (5%) |
| | | Timing Diagram (5%) |

Out of the 85% for Pre-Lab and Lab.: Lab. 1, 2, 3, 4, 5, 6 are 10% each. Lab. 7 is 25%.

Laboratory report is due one week after the lab is completed. A sample lab report and the grading rubric is available in moodle.
The quizzes will be conducted during the lecture.

**Tentative Schedule**

| **Meeting** | **Experiment** |
|---|---|
| 1 | 1 |
| 2 | 1 |
| 3 | 2 |
| 4 | 3 Quiz 1 |
| 5 | 4 |
| 6 | 4 |
| 7 | 5 |
| 8 | 5 |
| 9 | 6 Quiz 2 |
| 10 | 6 |
| 11 | 7 |
| 12 | 7 |
| 13 | 7 |
| 14 | 7 |
| 15 | Final |