ECE353 Course Syllabus

1. **Course number and name: ECE 353**: Computer Architecture and Organization

2. **Credits and contact hours:** 3 credit hours, 3 contact hours

3. **Instructor's or course coordinator's name:** John Carpinelli

4. **Text book, title, author and year**
   Computer Systems Organization and Architecture, Addison-Wesley, John D.
   Carpinelli, Boston, MA, 2001, ISBN # 0-201-61253-4.

5. **Specific course information**
   a. brief description of the content of the course (Catalog Description)
      - This course emphasizes the hardware design of computer systems.
      - Topics include register transfer logic, central processing unit design, microprogramming, ALU design, pipelining, vector processing, micro-coded arithmetic algorithms, I/O organization, memory organization and multiprocessing.

   b. prerequisites or co-requisites
      - ECE 252

   c. indicate whether a required, elective, or selected elective
      Required

6. **Specific goals for the course**
   - The students are able to design the instruction set architecture for a processor to meet specific computer requirements. (c,e)
   - The students are able to evaluate the tradeoffs in the design of an instruction set architecture and the processor that implements it. (a,e)
   - The students are able to design a system to meet a given specification using register transfer language. (a,e)
   - The students are able to design a basic CPU given the instruction set architecture using either hardwired or microcoded control. (e)
   - The students are able to design a hierarchical memory system to meet a given specification. (e)
   - The students are able to design an I/O system to meet a given specification.(e)

7. **Brief list of topics to be covered**

Chapter	Topic	Week
3	Instruction Set Architectures	1
4	Basic Computer Organization	2

5	Register Transfer Languages	3,4
6	CPU Design - Hardwired Control**, *Test #1***	4,5
7	Microsequencers Control Unit Design	6,7
8	Computer Arithmetic	8,9
9	Memory Organization	10,11
10	I/O Organization, *Test #2*	11,12
11	RISC Processing	13
12	Parallel Processing	14

NOTE: Final Exam will be held during the week of December 13-19.
2013.

8. Student outcomes addressed by the course

- an ability to apply knowledge of mathematics, science, and engineering
- an ability to design a system, component, or process to meet desired needs within realistic
- an ability to identify, formulate, and solve engineering problems
- a recognition of the need for, and an ability to engage in life-long learning
- a knowledge of contemporary issues
- an ability to communicate effectively

9. Grading

- Homework and class participation: 20%
- 2 tests @ 25%:   50%
- Final exam: 30%

10. Course Policies

- Homework submission: Written homework assignments are due at the beginning of the class on the due date. No late homework will be accepted.
- Intellectual Dishonesty: All submitted assignments would consist of only the student's own work. Seeking help from fellow students is encouraged; however, never ask others to do your work nor let others copy yours. If copying is suspected everybody involved will receive a ZERO for the assignment.

11. NJIT Honor Code

The NJIT Honor Code will be strongly upheld. Violation will be referred to the Dean of Students for disciplinary action.