

ECE 495 Fall 2018

Computer Engineering Design Laboratory

Course Description: This course emphasizes hardware design and debugging. Topics include combinational and sequential logic design using CAD tools, VHDL, and design based upon PLA/PLD.

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Lecture/Laboratory meet at: M 1:00pm – 2:20pm (FMH 408) / R 8:30am – 12:50pm (LSEC 302B), R 1:00pm – 5:20m (LSEC 302B)

Office hours: W 11:00am-12:00pm or by appointment

Prerequisites: ECE 353 and ECE 394

Recommended Text: J. Knoots, E. Hou, Laboratory and Supplementary Notes, ECE 495: Computer Engineering Design Laboratory, Ver. 3.0, ECE Dept. 2007. **This manual is for reference only. Refer to lecture notes for up to date information.**
You will also need the Lab kit for
ECE 394. Any VHDL book.

Honor code: The NJIT honor code will be upheld and that any violations will be brought to the immediate attention of the Dean of Students.

Course Learning Outcomes (CLO):

Student should be able to

1. design sequential circuits (using EEPROM) that meets a given design specification
2. use CAD tools to design, implement and verify their hardware system designs.
3. design hardware system and write VHDL program to implement them.
4. write lab reports documenting the results of the lab experiments.

Relevant ABET Student Outcomes:

- (1) an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1, 2, 3)
- (2) an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (CLO 1, 2, 3)
- (3) an ability to communicate effectively with a range of audiences (CLO 4)
- (6) an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLO 1, 2, 3)

Grading Policy

Lab assessment:	5%	
Quizzes & Final:	20%	
Lab.:	60%	
Demo	40%	Writing (10%)
Report	20%	Logic Diagram, Wiring Diagram, Software/Code comments, Timing Diagram, etc. (10%)
Pre-Lab:	15%	Logic Diagram/Tables, Wiring Diagram, Software/Code, Timing Diagram, etc.

Out of the 75% for Pre-Lab and Lab.: Lab. 1, 3, 4, 5, 6 are 10% each; Lab. 2 is 5%. Lab. 7 is 20%.

Laboratory report is due one week after the lab is completed. A sample lab report and the grading rubric are available in moodle.

The quizzes will be conducted during the lecture.

Tentative Schedule

Meeting	Experiment
1	1
2	1
3	2
4	3 Quiz 1
5	3
6	4
7	4
8	5
9	5 Quiz 2
10	6
11	6
12	7
13	7
14	7
15	Final