

## ECE 459 Syllabus

### ECE 459-002 Advanced Computer Systems Design Lab

**2.0 credits**

**Instructor:** Timothy Steele. **E-mail:** [timothy.steele@njit.edu](mailto:timothy.steele@njit.edu) **Phone:** 973-596-3539

**Office Hours:** Monday 9:00-10:00 AM, or by appointment (e-mail). Room ECEC 310

**Textbook:** S.G. Ziavras, *ECE 459: Computer Systems Design Laboratory, Version 2*, Help notes and part of the syllabus co-developed with S.F. Beldianu.

**Course Description:** Design laboratory component of the advanced computer systems technical track offered to CoE majors in the senior year. Experiments emphasize advanced CPU design concepts, such as RISC approaches and exception handling, multiprocessor and systolic array computers, and FPGAs. Develop software programs to test the capabilities of these hardware designs.

**Prerequisite:** ECE 451, ECE 495

**Corequisite:** ECE 452

#### Specific course learning outcomes

Upon successfully completing the course a student is able to:

#	Outcome
1	Write complex programs in MIPS assembly language.
2	Design a program to do matrix multiplication.
3	Design a program to do a recursive process.
4	Write complex functions in VHDL and implement them for an FPGA.
5	Design a systolic array for numerical processing.
6	Design a shared memory dual core system in an FPGA.
7	Design a simple cpu core with support for external interrupts in an FPGA.

#### General student outcomes addressed by the course

(1) an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (1-7)

(2) an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors. (1-7)

#### Schedule:

Week	Topics	Book Sections
1-2	Introduction, Experiment 1: Matrix Multiplication	
3-4	Experiment 2: Recursion	
5-7	Experiment 3: Systolic Array Processing	

8-10	Experiment 4: Shared Memory Multi-processor	
11-14	Experiment 5: CPU Design with External Interrupts	

**Grading Policy**

1. Reports 25%
2. Laboratory Effort 25%
3. Presence in Laboratory 25%
4. Quality of Results (Presentation) 25%

**Honor Code**

The NJIT Honor Code will be upheld, and any violation will be brought to the immediate attention of the Dean of Students.