Ph.D. Dissertation Proposal Defense

Candidate: Nandakumar Sasidharan Rajalekshmi
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Venue: ECEC 202
Title: On-chip Supervised Training of Spiking Neural Networks

Abstract

The goal of Neuromorphic engineering is to mimic the architecture of the human brain to design and develop intelligent computing hardware. Deep neural networks which are extensively used in today's machine learning applications such as social media analysis, autonomous navigation, business forecasting etc., uses second generation model of artificial neurons, which does not capture the temporal dynamics of biological neurons. Spiking neural networks (SNNs) on the other hand, aims to capture the time-based information encoding and processing capability of biological neurons. The high computational efficiency of the brain is attributed to its highly parallel architecture, local learning and efficient data encoding in the spike domain. It is estimated that the overall power budget of the human brain is only about 20 W. One of the major challenges of today's machine learning algorithms is the huge amount of time needed for training the networks. Dedicated implementations of these algorithms in hardware are prohibitively expensive, both in terms of area and power. Hence, there are world-wide efforts to build special purpose computing chips in order to accelerate the performance of machine learning algorithms. It is believed that owing to the natural sparsity properties of spiking neurons, the implementation of machine learning algorithms that uses SNN architecture will be more power efficient and suitable for mobile computing and IoT platforms.

The aim of our research is to devise the optimal architecture to realize bio-mimetic spiking neural networks, based on the constraints imposed by nanoscale hardware devices. We are exploring emerging memories capable of non-volatile gradual conductance change such as resistive random access memory (RRAM) and phase change memory (PCM) to mimic biological synapses. We are developing a physics based switching model for RRAM and its phenomenological model for spike timing dependent plasticity (STDP) behavior to analyze the efficiency of spike based learning algorithms. We are also using a PCM device array platform (currently available at IBM Zurich laboratories) to implement these algorithms. A new insulator-metal-transition based device has shown unique bio-mimetic spiking behavior; this device model is being analyzed to efficiently implement spike coding schemes suited for computation and learning. Summarizing these studies, I will discuss future directions for this research project.

Committee members:
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Relevant Publications:

1. S. R. Nandakumar, M. Minvielle, S. Nagar, C. Dubourdieu, and B. Rajendran,"A 250 mV $Cu/SiO_2/W$ Memristor with Half-Integer Quantum Conductance States" Nano Lett., p. acs. nanolett.5b04296, 2016.

2. S. R. Nandakumar and B. Rajendran, "Physics-based switching model for $Cu/SiO_2/W$ quantum memristor," in 2016 74th Annual Device Research Conference (DRC), 2016, vol. 16, no. 973, pp. 1-2.

3. S. R. Nandakumar and B. Rajendran, "Verilog-A compact model for a novel $Cu/SiO_2/W$ quantum memristor," in 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2016, no. 973, pp. 169-172.

4. S. R. Nandakumar, et al, Supervised training on differential-multi-PCM synaptic array, Manuscript under preparation.