

## **Ph.D. Dissertation Defense**

### **Soft-Error Resilient On-Chip Memory Structures**

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#### **Abstract**

Soft errors induced by energetic particle strikes in on-chip memory structures, such as L1 data/instruction caches and register files, have become an increasing challenge in designing new generation reliable microprocessors. Due to their transient/random nature, soft errors cannot be captured by traditional verification and testing process due to the irrelevancy to the correctness of the logic. Applying techniques such as hardware triple modular redundancy (TMR) or N-modular redundancy (NMR) for addressing soft errors might not be acceptable to commercial computer systems in most market segments. This dissertation is thus focusing on the reliability characterization and cost-effective reliable designs of on-chip memories against soft errors.

Due to various performance, area/size, and energy constraints in various target systems, many existing unoptimized protection schemes on cache memory structures may eventually prove significantly inadequate and ineffective. This work develops new lifetime models for data and tag arrays residing in both the data and instruction caches. Those models facilitate the characterization of cache vulnerability of stored items at various lifetime phases. The design methodology is further exemplified by the proposed reliability schemes targeting at specific vulnerable phases. For enhancing the reliability of the tag array of on-chip caches, a tag replication buffer (TRB) design is proposed to exploit the address locality of memory accesses for keeping tag replicas of recently accessed cachelines. Furthermore, in order to design the reliable systems in the changing operating environments (error rates), this work explores the design of a self-adaptive reliable data cache that dynamically adapts its employed reliability schemes to maintain a target reliability. Besides the data/instruction caches, protecting the register file and its data buses is crucial to reliable computing in high-performance microprocessors. This work proposes to exploit narrow-width register values, which present the majority of the generated values, for making a duplicate of the value within the same data item. This in-register duplication (IRD) eliminates the requirement for additional copy registers. By integrating the proposed reliable designs in data/instruction caches and register files, the vulnerability of the entire microprocessor will be dramatically reduced. The new lifetime model, the self-adaptive design and the narrow-width value duplication scheme proposed in this work can also provide the guidance to architects for the future highly efficient reliable system design.

#### **Committee Members:**

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